What is claimed is:

1. A clock distortion detector, comprising:

a first input for receiving a first clock signal;

a second input for receiving a second clock signal; and

at least one mirror delay element.

2. The clock distortion detector of claim 1, comprising:

a first mirror delay element, comprising two inputs and two outputs; and

a second mirror delay element, comprising two inputs and two outputs,

wherein a second output of the first mirror delay element is coupled with a first input of the second mirror delay element, and

a first output of the second mirror delay element is coupled with a second input of the first mirror delay element.

3. The clock distortion detector of claim 2, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

4. The clock distortion detector of claim 2, wherein the first and the second mirror delay elements each additionally comprise two control inputs.

5. The clock distortion detector of claim 4, wherein the first clock signal is fed to the respective first

control inputs, and the second clock signal is fed to the respective second control inputs.

6. The clock distortion detector of claim 5, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

7. The clock distortion detector of claim 2, further comprising a test device coupled to a first input of the first mirror delay element.

8. The clock distortion detector of claim 7, wherein the test device additionally is coupled to a first output of the first mirror delay element.

9. The clock distortion detector of claim 8, wherein the test device is adapted to compare the signal input into the first input of the first mirror delay element with the signal output at the first output of the first mirror delay element.

10. A clock distortion detection method, comprising:

applying a clock signal to a control input of a first mirror delay element; and

applying the clock signal to a control input of a second mirror delay element,

wherein a signal output by the first mirror delay element is applied to the second mirror delay element, and

a signal output by the second mirror delay element is applied to the first mirror delay element.